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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/942,038	08/30/2001	Yoshihiro Mori	0819-0637	7302

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EXAMINER

DOTY, HEATHER ANNE

ART UNIT	PAPER NUMBER
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2813

DATE MAILED: 03/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

4A

Office Action Summary	Application No.		Applicant(s)	
	09/942,038		MORI ET AL.	
	Examiner		Art Unit	
	Heather A. Doty		2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
 - If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
 - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
 - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 19 November 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-9 and 38-60 is/are pending in the application.
- 4a) Of the above claim(s) 1-9 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 38-60 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 29 October 2002 and 30 August 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date <u>8/30/01, 6/10/03</u> | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Information Disclosure Statement

Portions of the information disclosure statement filed 6/10/03 fail to comply with 37 CFR 1.98(a)(2). Specifically, the examiner is unable to locate in the application image file the non-patent literature "NOTICE OF REASONS OF REJECTIONS (DATED MARCH 11, 2003)." It appears the document did not survive the transition from the paper file system to the application's image file ("the file"). Applicant is respectfully requested to resubmit the document for proper consideration of current record.

Additionally, a scanned copy of Japanese patent 11-111930 (04-23-1999) is missing from the file. The examiner has located a machine-translated copy of this patent and is submitting it with this office action to be scanned and added to the file. The information in this document has been considered by the current examiner.

Finally, a scanned copy of Japanese patent 11-074488 (03/16/1999) included in the information disclosure statement filed 8/30/01 is also missing from the file. The examiner has located a machine-translated copy of this patent and is submitting it with this office action to be scanned and added to the file. The information in this document has been considered by the current examiner.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless – (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 38, 39, 46, 48-50, and 52-60 are rejected under 35 U.S.C. 102(b) as being anticipated by Takeshi (JP 11-150245, 6/02/99).

With respect to claim 38, Takeshi teaches a method for fabricating a semiconductor device, the method comprising the steps of: a) forming a metal lower electrode on a substrate (paragraph 16; **12** in drawing 2); b) annealing the metal lower electrode in a reducing atmosphere that contains impurity atoms (paragraph 17); c) forming a capacitive insulating film on the metal lower electrode after the step b) (paragraph 18; **13** in drawing 2); and d) forming an upper electrode on the capacitive dielectric film (paragraph 18; **14** in drawing 2), wherein the impurity atoms are introduced into the metal lower electrode in the step b), which is inherent, as admitted by applicant on page 8, lines 18-20 and page 12, line 16 to page 15, line 2 (see MPEP 2112).

With respect to claim 39, Takeshi teaches the method of claim 38, wherein the impurity atoms are hydrogen atoms (paragraph 17).

With respect to claim 46, Takeshi teaches the method of claim 38, wherein the metal electrode is made of a noble metal (paragraph 2; claim 4).

With respect to claims 48-50, Takeshi teaches the method of claim 38, wherein the metal lower electrode is composed of Pt, Ir, or Ru (Takeshi, claim 4).

With respect to claim 52, Takeshi teaches the method of claim 38, wherein the capacitive dielectric film is an insulating film made of an oxide (Takeshi, claim 3).

With respect to claim 53, Takeshi teaches the method of claim 38, wherein the capacitive dielectric film is composed of BST (Takeshi, claim 2).

With respect to claim 54, Takeshi teaches the method of claim 38, wherein the capacitive dielectric film is composed of SBT (Takeshi, claim 3).

With respect to claim 55, Takeshi teaches the method of claim 38, wherein the capacitive dielectric film is composed of PZT (abstract).

With respect to claim 56, Takeshi teaches the method of claim 38, wherein the capacitive dielectric film is composed of Ta₂O₅ (Takeshi, claim 2).

With respect to claim 57, Takeshi teaches the method of claim 38, wherein the metal lower electrode is composed of Ru (Takeshi, claim 4), and the capacitive dielectric film is composed of Ta₂O₅ (Takeshi, claim 2).

With respect to claim 58, Takeshi teaches the method of claim 38, wherein the metal lower electrode is composed of Ir (Takeshi, claim 4), and the capacitive dielectric film is composed of SBT (Takeshi, claim 3).

With respect to claim 59, Takeshi teaches the method of claim 38, wherein the metal lower electrode is composed of Ir (Takeshi, claim 4), and the capacitive dielectric film is composed of PZT (abstract).

With respect to claim 60, Takeshi teaches the method of claim 38, wherein the annealing process is performed at a temperature of 400° C or more (paragraph 17).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claim 40 is rejected under 35 U.S.C. 103(a) as being unpatentable over Takeshi (JP 11-150245, 6/02/99) in view of Schrems et al. (US 2002/0025622 A1).

With respect to claim 40, Takeshi teaches the method of claim 38 (note 35 U.S.C. 102(b) rejection above), but does not expressly teach that the annealing process is performed in an argon atmosphere containing hydrogen.

Schrems et al. teaches a method of fabricating a capacitor comprising the step of annealing the bottom electrode in an argon atmosphere containing hydrogen (paragraphs 0028 and 0035).

Therefore, at the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the method for fabricating a semiconductor device as in

Takeshi and in claim 38 by annealing the lower electrode in an argon atmosphere containing hydrogen, as in Schrems et al. The motivation for doing so at the time of invention would have been to incorporate hydrogen into the lower electrode to enable the use of physically thinner dielectric layers, as expressly taught by Schrems et al. (paragraph 0032).

Claim 41 is rejected under 35 U.S.C. 103(a) as being unpatentable over Takeshi (JP 11-150245, 6/02/99) in view of Dennison et al. (U.S. 5,162,248).

With respect to claim 41, Takeshi teaches the method of claim 38 (note 35 U.S.C. 102(b) rejection above), but does not expressly teach forming an insulating film on the substrate and forming a recess on the insulating film before the step a).

Dennison teaches a method for fabricating a semiconductor device comprising the steps of forming an insulating film on the substrate (**21** in Fig. 2; column 4, lines 45-47) and forming a recess on the insulating film (**22** in Fig. 2; column 4, lines 60-61, 64-67) before forming a lower electrode on the substrate, wherein the lower electrode is formed in the recess (**51** in Fig. 5; column 4, lines 67-68; column 5, lines 41-43).

Therefore, at the time of invention, it would have been obvious to a person of ordinary skill in the art to modify the method of forming a capacitor as taught by Takeshi and as in claim 38 by forming an insulating film over the substrate and forming a recess on the insulating film before forming the lower electrode on the substrate, wherein the lower electrode is formed in the recess in the step b), as taught by Dennison. The motivation for doing so at the time of invention would have been to provide a support form for the bottom electrode, as expressly taught by Dennison (column 4, lines 64-67).

Claim 42 is rejected under 35 U.S.C. 103(a) as being unpatentable over Takeshi (JP 11-150245, 6/02/99) in view of Schrems et al. (US 2002/0025622 A1) as applied to claim 40 above, and further in view of Dennison et al. (U.S. 5,162,248).

Together Takeshi and Schrems et al. teach the method of claim 40 (note 35 U.S.C. 103(a) rejection above), but do not expressly teach the steps of forming an insulating film on the substrate and forming a recess in the insulating film before the step a), wherein the metal lower electrode is formed in the recess in the step b).

Dennison et al. teaches a method for fabricating a semiconductor device comprising the steps of forming an insulating film on the substrate (**21** in Fig. 2; column 4, lines 45-47) and forming a recess on the insulating film (**22** in Fig. 2; column 4, lines 60-61, 64-67) before forming a lower electrode on the substrate, wherein the lower electrode is formed in the recess (**51** in Fig. 5; column 4, lines 67-68; column 5, lines 41-43).

Therefore, at the time of invention, it would have been obvious to a person of ordinary skill in the art to modify the method of forming a capacitor as taught by Takeshi and Schrems et al. and as in claim 40 by forming an insulating film over the substrate and forming a recess on the insulating film before forming the lower electrode on the substrate, wherein the lower electrode is formed in the recess in the step b), as taught by Dennison. The motivation for doing so at the time of invention would have been to provide a support form for the bottom electrode, as noted above and expressly taught by Dennison (column 4, lines 64-67).

Claim 43 is rejected under 35 U.S.C. 103(a) as being unpatentable over Takeshi (JP 11-150245, 6/02/99) in view of Kashihara et al. (U.S. 5,382,817).

With respect to claim 43, Takeshi teaches the method of claim 38 (note 35 U.S.C. 102(b) rejection above), but does not teach that the metal lower electrode has a thickness of 100 nm or less at the thinnest part thereof.

Kashihara et al. teaches a method of forming a capacitor wherein the metal lower electrode has a thickness of 50-100 nm (column 24, claim 3).

Therefore, at the time of the invention, it would have been obvious to modify the method of forming a semiconductor device as taught by Takeshi and as in claim 38 by making the metal lower electrode with a thickness of 100 nm or less at the thinnest part thereof, as taught by Kashihara et al. The motivation for doing so at the time of invention would have been to provide a semiconductor device with sufficient capacity for memory storage as the device is miniaturized, as taught by Kashihara et al. (column 6, lines 45-48).

Claims 44, 45, and 47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takeshi (JP 11-150245, 6/02/99) in view of Kim et al. (6,580,111).

With respect to claim 44, Takeshi teaches the method of claim 38 (note 35 U.S.C. 102(b) rejection above), but does not expressly teach that the capacitive dielectric film is formed in an oxidizing atmosphere in the step c).

Kim et al. teaches a method for fabricating a capacitor wherein the capacitive dielectric film is formed in an oxidizing atmosphere (column 6, lines 24-27).

Therefore, at the time of invention, it would have been obvious to a person of ordinary skill in the art to modify the method of fabricating a semiconductor device as taught by Takeshi and as in claim 38 by forming the capacitive dielectric film in an oxidizing atmosphere, as taught by Kim et al. The motivation for doing so at the time of the invention would have been to form the capacitive layer of a high-dielectric material, as taught by Kim et al. (column 2, line 39).

With respect to claim 45, Takeshi teaches the method of claim 38 (note 35 U.S.C. 102(b) rejection above), but does not expressly teach crystallizing the capacitive dielectric film by a heat treatment after the step c) and before the step d).

Kim teaches a method of forming a capacitor comprising the step of crystallizing the capacitive dielectric film by a heat treatment after forming the capacitive dielectric film and before forming the upper electrode (column 2, lines 48-51; column 6, lines 39-42). The motivation for doing so at the time of the invention would have been to improve the electrical characteristics of the capacitive dielectric film, as expressly taught by Kim et al. (column 2, lines 48-51).

With respect to claim 47, Takeshi teaches the method of claim 38 (note 35 U.S.C. 102(b) rejection above), but does not teach that the lower electrode is made of a refractory metal.

Kim et al. teaches a method of fabricating a capacitor wherein the lower electrode is made of a refractory metal (column 2, lines 36-37).

Therefore, at the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the method of forming a semiconductor device as

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taught by Takeshi and in claim 38 by making the lower electrode of a refractory metal, as taught by Kim et al. The motivation for doing so at the time of the invention would have been because refractory metals are easy to deposit and pattern (column 2, lines 66-67).

Claim 51 is rejected under 35 U.S.C. 103(a) as being unpatentable over Takeshi (JP 11-150245, 6/02/99) in view of Park et al. (U.S. 6,180,447).

With respect to claim 51, Takeshi teaches the method of claim 38 (note 35 U.S.C. 102(b) rejection above), but does not expressly teach that the lower electrode is composed of Rh.

Park et al. teaches a method for fabricating a capacitor wherein the metal lower electrode is composed of Rh (column 1, line 46).

Therefore, at the time of invention, it would have been obvious to a person of ordinary skill in the art to modify the method of forming a semiconductor device as taught by Takeshi and as in claim 38 by forming the lower electrode of Rh, as taught by Park et al. The motivation for doing so at the time of invention would have been because Rh has excellent oxidation resistance, as expressly taught by Park et al. (column 1, lines 47-48).

Response to Arguments

Applicant's arguments with respect to claims 38-60 have been considered but are moot in view of the new grounds of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Heather A. Doty, whose telephone number is 571-272-8429. The examiner can normally be reached on M-F, 8:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr. can be reached on 571-272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

had


ERIK KIELIN
PRIMARY EXAMINER